CLAIMS

1. An apparatus comprising:

   a memory cell;

   ground control circuitry coupled to the memory cell to programmably control a voltage at a first ground;

   first circuitry coupled to the memory cell to provide a first voltage to the memory cell during a first period, the first voltage referenced to the first ground; and

   second circuitry coupled to the memory cell to provide a second voltage to memory cell during a second period, the second voltage referenced to a second ground different from the first ground.

2. The apparatus of claim 1 wherein the ground control circuitry comprises a plurality of transistors coupled in parallel between the second ground and the first ground.

3. The apparatus of claim 2 wherein the plurality of transistors coupled in parallel comprise MOSFETs.

4. The apparatus of claim 2 wherein the plurality of transistors coupled in parallel comprise binary weighted transistors.

5. The apparatus of claim 1 wherein the first period comprises a period of non-access of the memory cell.

6. The apparatus of claim 1 wherein the second ground comprises a system ground.

7. The apparatus of claim 1 further comprising a regulator circuit coupled to the ground control circuitry.

8. The apparatus of claim 7 wherein the regulator circuit comprises:

a comparator coupled to the first circuitry;

a reference voltage coupled to the comparator; and

a counter coupled to the comparator and the ground control circuitry.

9. The apparatus of claim 8 wherein a voltage divider provides the reference voltage.

10. An apparatus comprising:

a memory cell coupled to a supply voltage;

ground control circuitry coupled to the memory cell to programmably control a voltage at a first ground.

11. The apparatus of claim 10 wherein the ground control circuitry comprises a plurality of MOSFET devices.

12. The apparatus of claim 11 wherein the plurality of MOSFET devices comprise binary weighted transistors.

13. A method comprising:

providing a first voltage to a memory cell during periods of activity of a memory cell, the first voltage referenced to a system ground; and

providing a second voltage to the memory cell during periods of inactivity of the memory cell, wherein second voltage resulting from a programmable ability to control a virtual ground.

14. The method of claim 13 wherein the first voltage is greater than the second voltage.

15. The method of claim 13 wherein a plurality of parallel MOSFETs facilitate the programmable ability to control a virtual ground.

16. An apparatus comprising:

a plurality of memory cells;

a plurality of ground control circuitries correspondingly coupled to the plurality of memory cells to provide a programmable ability to correspondingly control voltages at a first plurality of grounds;

a first plurality of circuitries correspondingly coupled to the plurality of memory cells to correspondingly provide a plurality of first voltages to the plurality of

memory cells, the plurality of first voltages correspondingly referenced to the first plurality of grounds wherein the plurality of first voltages are correspondingly applied to the plurality of memory cells during corresponding access periods of the memory cells; and

a second plurality of circuitries correspondingly coupled to the plurality of memory cells to correspondingly provide a plurality of second voltages to the plurality of memory cells, the plurality of second voltages correspondingly referenced to a second plurality of grounds wherein the plurality of second voltages are corresponding applied to the plurality of memory cells during corresponding non-access periods of the memory cells.

17. The apparatus of claim 16 wherein at least one of the second plurality of grounds comprises a system ground.

18. The apparatus of claim 16 wherein at least one of the first plurality of grounds comprises a single programmable virtual ground.

19. The apparatus of claim 16 wherein at least one of the plurality of ground control circuitries comprises a plurality of MOSFETs coupled in parallel between the respective second ground and the respective first ground.

20. A system comprising:

a processor including;

a circuit comprising:

a plurality of on-chip memory cells;

a plurality of ground control circuitries correspondingly coupled to the plurality of memory cells to facilitate a programmable ability to correspondingly control voltages of a first plurality of grounds;

a first plurality of circuitries correspondingly coupled to the plurality of memory cells to correspondingly provide a plurality of first voltages to the plurality of memory cells, the plurality of first voltages correspondingly referenced to the first plurality of grounds wherein the plurality of first voltages are correspondingly applied to the plurality of memory cells during access periods of the memory cells; and

a second plurality of circuitries correspondingly coupled to the plurality of memory cells to correspondingly provide a plurality of second voltages to the plurality of memory cells, the plurality of second voltages correspondingly referenced to a second plurality of grounds wherein the plurality of second voltages are correspondingly applied to the plurality of memory cells during non-access periods of the memory cells;

a networking interface;

an off-chip memory configured to store data; and

a bus coupled to the processor, networking interface and memory.

21. The system of claim 20 further comprising a regulator circuit coupled to the plurality of ground control circuitries.

22. The system of claim 21 wherein the regulator circuit comprises:

a comparator coupled to the plurality of first circuitries;

a reference voltage coupled to the comparator; and

a counter coupled to the comparator and the plurality of ground control circuitries.

23. The system of claim 22 wherein a voltage divider provides the reference voltage.

24. The system of claim 20 wherein at least one of the second plurality of grounds comprises a system ground.

25. The system of claim 20 wherein at least one of the first plurality of grounds comprises a single programmable virtual ground.